Having thus described the invention, it is now claimed:

1. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a first processing system;

storing the received data into a first memory device; and

executing a program instruction on an associated processor to transfer at least a portion of the stored data to a second memory device.

2. A data transfer method according to claim 1, wherein said method further comprises:

transferring at least a portion of the data stored in said second memory device to a third memory device, wherein said second processing system operates upon the data stored in said third memory device.

3. A data transfer method according to claim 1, wherein said first memory device is a FIFO memory device.

4. A data transfer method according to claim 1, wherein said third memory device is a FIFO memory device.

5. A data transfer method according to claim 1, wherein method further comprises byte-aligning the data stored in said first memory device.

6. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving data from a first processing system;

storing the received data into a first memory device;

transferring the stored data to a second memory device; and

executing a program instruction on an associated processor to store at least a portion of the data stored in the second memory device to a third memory device.

7. A data transfer method according to claim 6, wherein said second processing system operates upon the data stored in said third memory device.

8. A data transfer method according to claim 6, wherein said first memory device is a FIFO memory device.

9. A data transfer method according to claim 6, wherein said third memory device is a FIFO memory device.

10. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a first processing means;

means for storing the received data into a first memory means; and

executing a program instruction on an associated processing means to transfer at least a portion of the stored data to a second memory means.

11. A system according to claim 10, wherein said system further comprises:

means for transferring at least a portion of the data stored in said second memory means to a third memory means, wherein said second processing means operates upon the data stored in said third memory means.

12. A system according to claim 10, wherein said first memory means is a FIFO memory device.

13. A system according to claim 10, wherein said third memory means is a FIFO memory device.

14. A system according to claim 10, wherein system further comprises means for byte-aligning the data stored in said first memory means.

15. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving data from a first processing means;

means for storing the received data into a first memory means;

means for transferring the stored data to a second memory means; and

means for executing a program instruction on an associated processor means to store at least a portion of the data stored in the second memory means to a third memory means.

16. A system according to claim 15, wherein said second processing means operates upon the data stored in said third memory means.

17. A system according to claim 15, wherein said first memory means is a FIFO memory device.

18. A system according to claim 15, wherein said third memory means is a FIFO memory device.

19. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a first processing system; and

an associated processing device for executing a program instruction to transfers at least a portion of the stored data to a second memory device.

20. A system according to claim 19, wherein said system further comprises hardware logic for transferring at least a portion of the data stored in said second memory device to a third memory device, wherein a second processing system operates upon the data stored in said third memory device.

21. A system according to claim 19, wherein said first memory device is a FIFO memory.

22. A system according to claim 19, wherein said third memory device is a FIFO memory.

23. A system according to claim 19, wherein said first memory device byte-aligns the data stored therein.

24. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing data received from a first processing system;

a second memory device for receiving the data stored in the first memory device; and

an associated processor for executing a memory read instruction to transfer at least a portion of the data stored in the second memory device to a third memory device.

25. A system according to claim 24, wherein said system further comprises a second processing system for operating upon the data stored in said third memory device.

26. A system according to claim 24, , wherein said first memory device is a FIFO memory.

27. A system according to claim 24, wherein said third memory device is a FIFO memory.

28. A data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising:

receiving a data packet from a first processing system, wherein said data packet includes a header portion and a data portion;

storing the received data packet into a first memory device;

transferring the data portion of the data packet from the first memory device to a third memory device; and

executing at least one program instruction on an associated processor to transfer the header portion to a second memory device.

29. A data transfer method according to claim 28, wherein a second processing system operates upon the data portion stored in said third memory device.

30. A data transfer method according to claim 28, wherein said first memory device is a FIFO memory device.

31. A data transfer method according to claim 28, wherein said third memory device is a FIFO memory device.

32. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

means for receiving a data packet from a first means for processing, wherein said data packet includes a header portion and a data portion;

means for storing the received data packet into a first memory means;

means for transferring the data portion to a third memory means; and

means for executing at least one program instruction on an associated processor to transfer the header portion to a second memory means.

33. A system according to claim 32, wherein a second means for processing operates upon the data portion stored in said third memory means.

34. A system according to claim 32, wherein said first memory means is a FIFO memory device.

35. A system according to claim 32, wherein said third memory means is a FIFO memory device.

36. A system for transferring data between two processing systems, wherein said two processing systems operate independently, said system comprising:

a first memory device for storing a data packet received from a first processing system, wherein said data packet includes a header portion and a data portion;

an associated processor for executing at least one program instruction on to transfer the header portion from the first memory device to a second memory device; and

hardware logic enabled by the associated processor to transfer the data portion from the first memory device to a third memory device.

37. A system according to claim 36, wherein said system further comprises a second processing system for operating upon the data stored in said third memory device.

38. A system according to claim 36, wherein said first memory device is a FIFO memory.

39. A system according to claim 36, wherein said third memory device is a FIFO memory.

40. A data processing system comprising:

a processor for transferring data to a memory location identified by an address stored in an address pointer register;

a FIFO memory for storing data; and

a first memory for storing data at a plurality of memory locations, each memory location identified by an address,

wherein the processor receives an instruction to transfer data from the FIFO memory to a memory location of the first memory identified by the address stored in the address pointer register, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a first parameter identifying the address pointer register, and a second parameter identifying the first memory.

41. A data processing system comprising:

a processor for transferring data from a memory location identified by an address stored in an address pointer register;

a first memory for storing data at a plurality of memory locations, each memory location identified by an address; and

a FIFO memory for storing data,

wherein the processor receives an instruction to transfer data from a memory location of the first memory identified by the address stored in the address pointer register to the FIFO memory, and automatically increments the address stored in the address pointer register to identify another memory location of the first memory, said instruction having a first parameter identifying the address pointer register, and a second parameter identifying the FIFO memory.